CLAIMS

What is claimed is:

1. A system, comprising:

an input that receives a synchronization signal having a frequency; and

an oscillator that provides a clock signal having a frequency, the oscillator adjusts the frequency of the clock signal based on a comparison of an indication of the frequency for the synchronization signal and a corresponding indication of the frequency for the clock signal.

2. The system of claim 1, further comprising

a first sampling system that provides a digital indication of the frequency for the synchronization signal; and

a second sampling system that provides a digital indication of the frequency for the clock signal, the oscillator adjusting the clock signal based on a comparison between the indication of frequency for the clock signal and the indication of the frequency for the synchronization signal.

3. The system of claim 2, wherein each of the first and second sampling systems performs respective oversampling at a rate that is at least four times that of the synchronization signal.

4. The system of claim 2, further comprising a comparator that compares the indication of the frequency for the clock signal and the indication of the frequency for the synchronization signal and provides a comparator output signal indicating desired adjustments to the frequency of the clock signal, the oscillator adjusting the frequency of the clock signal based on the comparator output signal.

5. The system of claim 1, further comprising:

a phase detector that compares the phase of the synchronization signal relative to the phase of the clock signal to provide a phase signal; and

a phase adjuster that delays the clock signal by an amount based on the phase signal.

6. The system of claim 5, further comprising an insertion loss compensator that provides a compensation signal indicative of insertion loss associated with the propagation of the synchronization signal to the input to facilitate phase adjustments to the clock signal.

7. The system of claim 1, further comprising an update control that sets a rate for updating the frequency of the clock signal.

8. The system of claim 7, wherein the update control sets the rate for updating the frequency of the clock signal based on at least one operating characteristic of an integrated circuit chip comprising the system.

9. The system of claim 1, further comprising a sampling system that comprises a delay network that provides plural output signals that capture different parts of the clock signal, the sampling system provides the corresponding indication of frequency for the clock signal based on the plural output signals.

10. The system of claim 1 implemented on an integrated circuit chip.

11. An integrated system comprising n integrated circuit chips, where n is a positive integer denoting the number of integrated circuit chips, at least n-1 of the integrated circuit chips comprising the system of claim 1, and at least one other of the integrated circuit chips providing the synchronization signal to the n-1 of the integrated circuit chips.

12. A system for synchronizing an integrated circuit (IC) chip, comprising:

a first sampling system that provides an indication of the frequency for a synchronization signal received at an input of the IC chip;

a second sampling system that provides an indication of frequency for an internally generated clock signal;

a comparator that provides a comparator signal based on a comparison of the indication of frequency for the clock signal and the indication of the frequency for the synchronization signal;

a controller that provides a control signal for implementing adjustments to the internally generated clock signal based on the comparator signal; and

an oscillator that provides the internally generated clock signal based on the control signal.

13. The system of claim 12, wherein at least one of the first and second sampling systems further comprises:

a delay network that provides plural output signals corresponding to different parts of a respective signal sampled by the at least one of the first and second sampling systems; and

a detection system that derives an indication of frequency for the respective signal sampled by the at least one of the first and second sampling systems based on the plural output signals.

14. The system of claim 12, wherein the indication of frequency for each of the synchronization signal and the clock signal comprises a respective digital value, the comparator providing the comparator output signal to indicate one of an incremental increase, an incremental decrease and a no-change condition for the clock signal.

15. The system of claim 12, further comprising:

a phase detector that compares the phase of the synchronization signal relative to the phase of the clock signal to provide a phase signal; and

a phase adjuster that delays the clock signal by an amount based on the phase signal for adjusting the phase of the clock signal to enable the system to provide a phase adjusted clock signal.

16. The system of claim 12, further comprising an insertion loss compensator that provides a compensation signal indicative of insertion loss associated with the propagation of the synchronization signal from an external source to the input of the IC chip to facilitate phase adjustments to the clock signal.

17. The system of claim 12, further comprising an update control that controls a rate at which the frequency of the clock signal is updated.

18. A synchronization system, comprising:

means for comparing an indication of frequency of an external reference signal and an indication of frequency of an internal clock signal; and

means for controlling oscillating means to provide the internal clock signal at a frequency based on the comparison of the external reference signal and the internal clock signal.

19. The system of claim 18, further comprising oscillating means for providing the internal clock signal based on control implemented by the means for controlling.

20. The system of claim 18, further comprising:

means for sampling the external reference signal to provide the indication of frequency of the external reference signal; and

means for sampling the internal clock signal to provide the indication of frequency of the internal clock signal.

21. The system of claim 18, further comprising:

means for comparing phase characteristics of the external reference signal and the internal clock signal to provide a phase signal; and

means for adjusting phase of the internal clock signal based on the phase signal.

22. The system of claim 18, further comprising means for compensating for insertion loss associated with propagation of the external reference signal from a source to an input of the system that receives the external reference signal.

23. The system of claim 18, further comprising means for updating the indication of frequency at an update rate to enable the means for controlling to implement adjustments to the frequency of the internal clock signal.

24. A method, comprising:

determining an indication of frequency for an input signal provided by an external source;

determining an indication of frequency for an internally generated signal; and

controlling an oscillator to provide the internally generated signal at a frequency based on a comparison of the indication of frequency for the input signal and the indication of frequency for the internally generated signal.

25. The method of claim 24 further comprising:

sampling the input signal to provide an input sample signal, the indication of frequency for the input signal being determined based on the input sample signal; and

sampling the internally generated signal to provide a clock sample signal, the indication of frequency for the internally generated signal being determined based on the clock sample signal.

26. The method of claim 25,

wherein the sampling of the input signal further comprises delaying the input signal to provide plural delayed signals corresponding different instances of the input signal based on which the indication of frequency for the input signal is determined; and

wherein the sampling of the internally generated signal further comprises delaying the internally generated signal to provide plural delayed signals corresponding to different instances of the internally generated signal based on which the indication of frequency for the internally generated signal is determined.

27. The method of claim 24, wherein the controlling further comprises providing at least one control signal to cause the oscillator to one of increase, decrease and not change the frequency of the internally generated signal.

28. The method of claim 24, further comprising:

comparing phase characteristics of the input signal and the internally generated signal to provide a phase signal; and

delaying the internally generated signal based on the phase signal to provide a phase adjusted internally generated signal.

29. The method of claim 24, further comprising implementing insertion loss compensation associated with propagation of the input signal from the external source to an input of an integrated circuit implementing the method.

30. The method of claim 24, further comprising controlling an update rate at which adjustments to the frequency of the internal clock signal are performed.

31. An integrated circuit chip configured to perform the method of claim 24.